What is claimed:

1. A semiconductor device having a non-volatile memory transistor having a split structure, the semiconductor device comprising:

a semiconductor substrate of a first conductivity type having a memory region;

a first well of a second conductivity type located in the memory region; and

a second well of a first conductivity type located in the first well, wherein the non-volatile memory transistor includes a source and drain that are located in the second well.

2. A semiconductor device having a non-volatile memory transistor according to claim 1, wherein the non-volatile memory transistor is operated using voltages selected from the group consisting of positive and negative voltages.

3. A semiconductor device having a non-volatile memory transistor according to claim 2, wherein the operation of the non-volatile memory transistor includes writing and/or erasing data in the non-volatile memory transistor.

4. A semiconductor device having a non-volatile memory transistor according to claim 2, wherein the semiconductor substrate is a p-type, the first well is an n-type, the second well is a p-type, and each of the pair of source and drain is an n-type.

5. A semiconductor device having a non-volatile memory transistor according to claim 2, wherein,

for writing data in the non-volatile memory transistor, a voltage in an opposite polarity is applied to the control gate, a voltage in one polarity is applied to one of the source and the drain, a voltage in the opposite polarity is applied to the other of the source and the drain, a voltage in the opposite polarity is applied to the second well, and a voltage in the one polarity is applied to the first well, and

for erasing data in the non-volatile memory transistor, a voltage in the one polarity is applied to the control gate, a voltage in the opposite polarity is applied to one of the source and the drain, a voltage in the opposite polarity is applied to the other of the source and the

drain, a voltage in the opposite polarity is applied to the second well, and a voltage in the one polarity is applied to the first well.

6. A semiconductor device having a non-volatile memory transistor according to claim 5, wherein

for writing data in the non-volatile memory transistor, a voltage of –3 V through –4 V is applied to the control gate, a voltage of +3 V through +4 V is applied to one of the source and the drain, a voltage of –5 V through –6 V is applied to the other of the source and the drain, a voltage of –5 V through –6 V is applied to the second well, and a voltage of +0.9 V through +3.3 V is applied to the first well, and

for erasing data in the non-volatile memory transistor, a voltage of +6V through +7 V is applied to the control gate, a voltage of –5 V through –6 V is applied to one of the source and the drain, a voltage of –5 V through –6 V is applied to the other of the source and the drain, a voltage of –5 V through –6 V is applied to the second well, and a voltage of +0.9 V through +3.3 V is applied to the first well.

7. A semiconductor device having a non-volatile memory transistor according to claim 3, wherein data is written in the non-volatile memory transistor by channel hot electrons, and data is erased by Fowler Nordheim Tunneling.

8. A semiconductor device having a non-volatile memory transistor according to claim 1, wherein the source and drain have an impurity concentration of $1 - 8 \times 10^{20}$ cm^{-3}, the second well has a surface impurity concentration of $0.5 - 5 \times 10^{16}$ cm^{-3}, and the second well has a peak impurity concentration of $1 - 4 \times 10^{17}$ cm^{-3}.

9. A semiconductor device having a non-volatile memory transistor according to claim 1, wherein the non-volatile memory transistor has a first gate insulation layer, a second gate insulation layer, a floating gate, a control gate and an intermediate insulation layer functioning as a tunnel insulation layer, wherein

the first gate insulation layer and the second gate insulation layer are located above the second well and between one of the pair of source and drain and the other of the pair of source and drain,

the floating gate is located above the first gate insulation layer,

the intermediate insulation layer is located above the floating gate, and

the control gate is located above the second gate insulation layer and rests on the floating gate through the intermediate insulation layer.

10. A semiconductor device having a non-volatile memory transistor according to claim 9, wherein

the semiconductor substrate includes first, second and third transistor regions including field effect transistors that operate at different voltage levels, wherein

the first transistor region includes a first voltage-type transistor that operates at a first voltage level,

the second transistor region includes a second voltage-type transistor that operates at a second voltage level, and

the third transistor region includes a third voltage-type transistor that operates at a third voltage level,

wherein the second voltage-type transistor has a gate insulation layer formed from at least two insulation layers, and includes an insulation layer that is formed in the same step in which a gate insulation layer of the first voltage-type transistor is formed.

11. A semiconductor device having a non-volatile memory transistor according to claim 10, wherein the third voltage-type transistor has a gate insulation layer formed from at least three insulation layers, and includes an insulation layer that is formed in the same step in which the gate insulation layer of the first voltage-type transistor is formed.

12. A semiconductor device having a non-volatile memory transistor according to claim 11, wherein the intermediate insulation layer of the non-volatile memory transistor is formed from at least three insulation layers, wherein first and second outermost layers of the three insulation layers respectively contact the floating gate and the control gate and are formed from a thermal oxidation method.

13. A semiconductor device having a non-volatile memory transistor according to claim 12, wherein the second outermost layer that contacts the control gate of the intermediate insulation layer is formed in the same step in which the gate insulation layer of the first voltage-type transistor is formed.

14. A semiconductor device having a non-volatile memory transistor according to claim 12, wherein the intermediate insulation layer includes an insulation layer between the first and the second outermost layers, that is formed by a CVD method.

15. A semiconductor device having a non-volatile memory transistor according to claim 14, wherein the silicon oxide layer is formed by the CVD method selected from a group consisting of a HTO (high temperature oxide) method and a TEOS (tetraethyl orthosilicate) method.

16. A semiconductor device having a non-volatile memory transistor according to claim 10, wherein the third voltage-type transistor has a gate insulation layer formed in the same step in which the intermediate insulation layer of the non-volatile memory transistor is formed, the gate insulation layer of the third voltage-type transistor being formed from at least three insulation layers.

17. A semiconductor device having a non-volatile memory transistor according to claim 10, wherein the first voltage-type transistor has a gate insulation layer having a film thickness of 3 – 13 nm.

18. A semiconductor device having a non-volatile memory transistor according to claim 10, wherein the second voltage-type transistor has a gate insulation layer having a film thickness of 4 – 15 nm.

19. A semiconductor device having a non-volatile memory transistor according to claim 10, wherein the third voltage-type transistor has a gate insulation layer having a film thickness of 16 – 45 nm.

20. A semiconductor device having a non-volatile memory transistor according to claim 10, wherein the non-volatile memory transistor has an intermediate insulation layer having a film thickness of 16 – 45 nm.

21. A semiconductor device having a non-volatile memory transistor according to claim 12, wherein the first outermost layer that forms the intermediate insulation layer of the non-volatile memory transistor has a film thickness of 5 – 15 nm, and the second outermost layer has a film thickness of 1 – 10 nm.

22. A semiconductor device having a non-volatile memory transistor according to claim 14, wherein the first outermost layer that forms the intermediate insulation layer of the non-volatile memory transistor has a film thickness of 5 – 15 nm, and the second outermost layer has a film thickness of 1 – 10 nm, and the silicon oxide layer formed between the first and the second outermost layers has a film thickness of 10 – 20 nm.

23. A semiconductor device having a non-volatile memory transistor according to claim 1, further comprising a selective oxide insulation layer formed by a selective oxidation on the floating gate.

24. A semiconductor device having a non-volatile memory transistor according to claim 10, wherein

the first voltage level that operates the first voltage-type transistor is 1.8 – 3.3 V,

the second voltage level that operates the second voltage-type transistor is 2.5 – 5 V, and

the third voltage level that operates the third voltage-type transistor is 10 – 15 V.

25. A semiconductor device having a non-volatile memory transistor according to claim 10, further comprising at least a flash-memory (flash EEPROM), wherein the flash-memory includes a memory cell array composed of non-volatile memory transistors and peripheral circuits formed therein.

26. A semiconductor device having a non-volatile memory transistor according to claim 25, further comprising another circuit region mixed together.

27. A semiconductor device having a non-volatile memory transistor according to claim 26, wherein the circuit region includes at least a logic.

28. A semiconductor device having a non-volatile memory transistor according to claim 25, wherein the first voltage-type transistor is included in at least one circuit selected from a group consisting of a Y-gate sense amplifier, an input/output buffer, an X-address decoder, a Y-address decoder, an address buffer and a control circuit.

29. A semiconductor device having a non-volatile memory transistor according to claim 25, wherein the second voltage-type transistor is included in at least one circuit selected from a group consisting of a Y-gate sense amplifier, an input/output buffer, an X-address decoder, a Y-address decoder and an interface circuit.

30. A semiconductor device having a non-volatile memory transistor according to claim 25, wherein the third voltage-type transistor is included in at least one circuit selected from a group consisting of a voltage generation circuit, an erase voltage generation circuit and a step-up voltage circuit.

31. A semiconductor device having a non-volatile memory transistor having a split-gate structure, the semiconductor device comprising:

a semiconductor substrate of a first conductivity type having a memory region;

a first well of a second conductivity type located in the memory region;

a second well of a first conductivity type located in the first well, wherein the non-volatile memory transistor includes a source and drain that are located in the second well; and

wherein the non-volatile memory transistor having a split gate structure comprises a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to act as a tunnel insulation layer, and a control gate, wherein the intermediate insulation layer is composed of at least three insulation layers, wherein a first layer of the three insulation layers contacts the floating gate, a third layer contacts the control gate, and a second layer is located between the first and third layers.

32. A semiconductor device having a non-volatile memory transistor having a split-gate structure, the semiconductor device comprising:

means for performing an data writing operation using a first voltage of a first polarity and a data erasing operation using a second voltage of a second polarity opposite from that of the first polarity;

said means including a substrate region selected from the group of a P-type substrate region and an N-type substrate region, a first well region of an opposite type than the substrate, a second well region of an opposite type than the first well, and a source and drain formed in the second well.